



Best Practices of Top-Gun Engineering Managers

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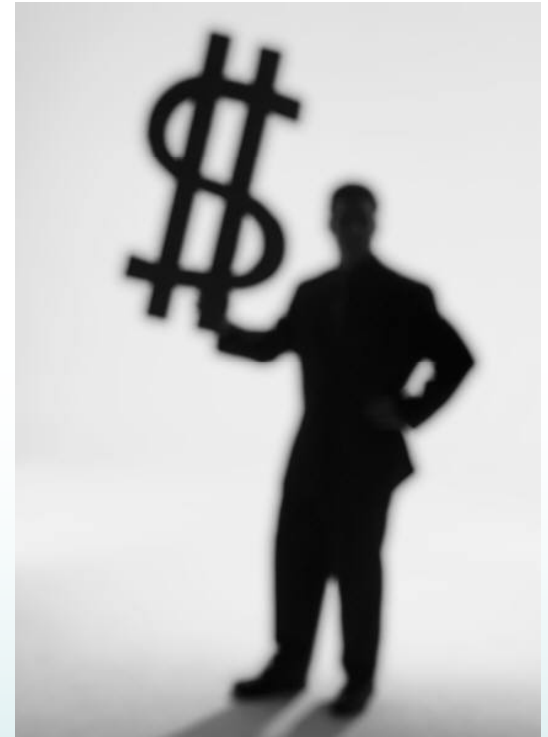
Agenda

- Introduction
- Eight Best Practices (20 minutes) – Alex Silbey
- Demonstration (20 minutes) – Shannon Johnston
- Q & A (15 minutes) – Alex and Shannon

Profile of “top-gun” IC engineering managers

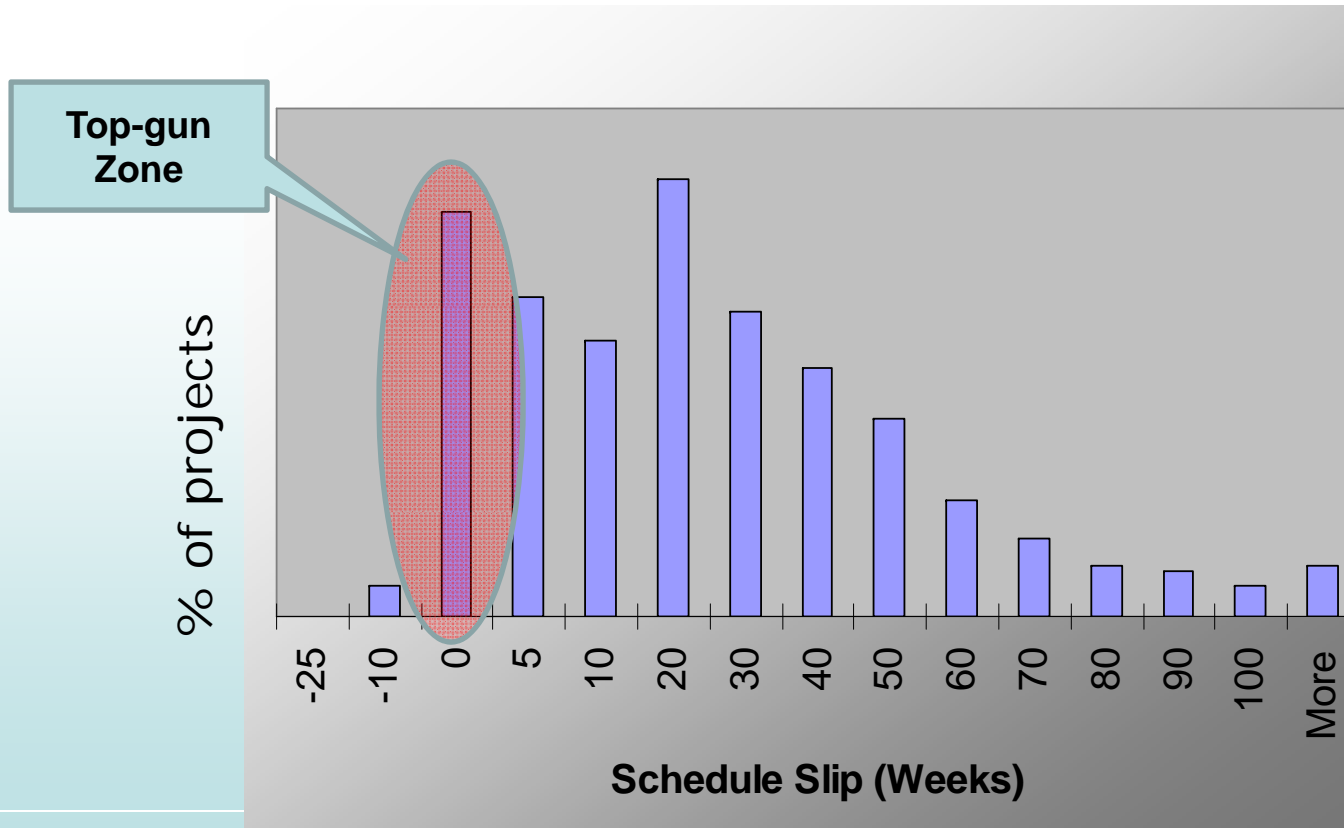
- Top-gun IC managers increase project performance over industry norms
 - 119% better project productivity
 - 40% shorter design cycle times
 - 50% fewer re-spins
 - 50% less schedule slip

- Better project performance translates directly into increased competitiveness



Schedule predictability—a candid view

- 60% of IC projects slip at least one quarter
- 16% of IC projects slip more than one year

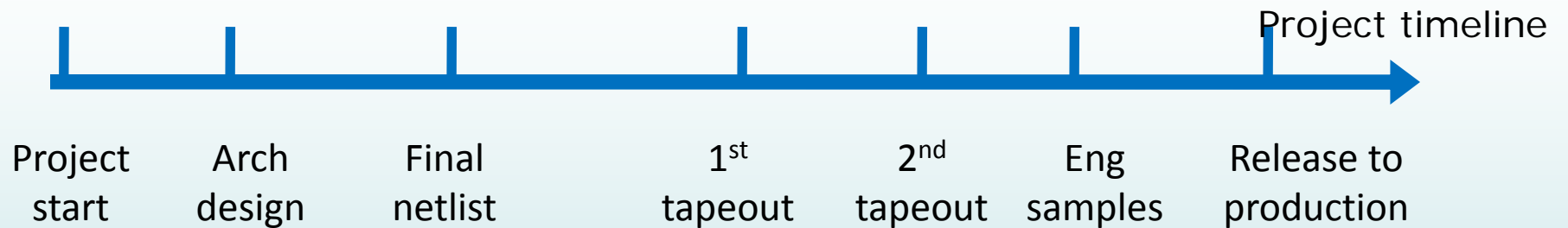


Lessons derived from extensive data analysis (NMX IC industry database)

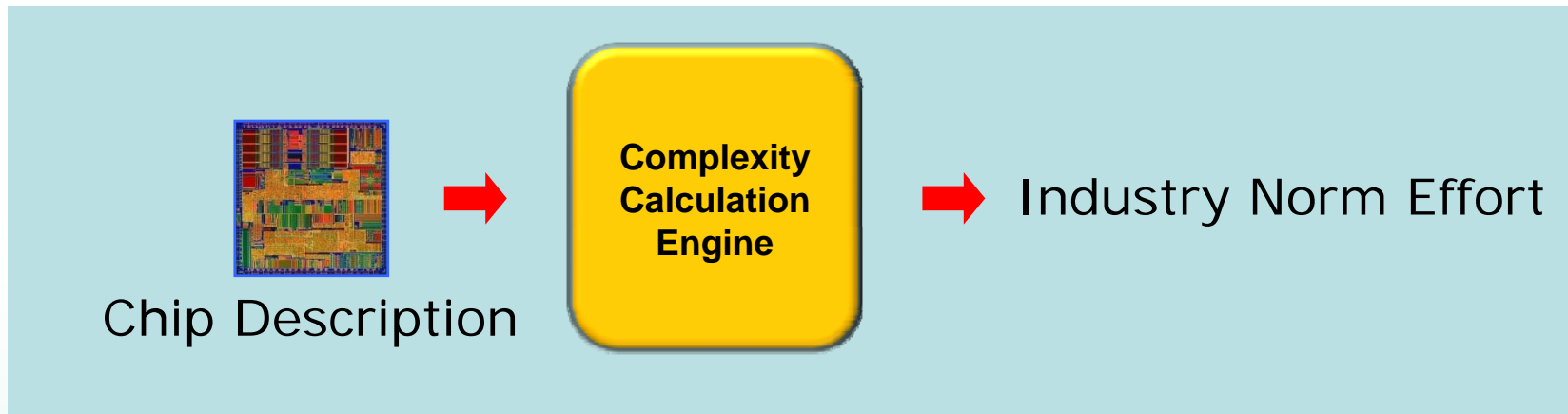


Where Top-guns Operate

- Top-gun managers use best practices throughout the project life cycle
- We define project duration from architectural description to release-to-volume



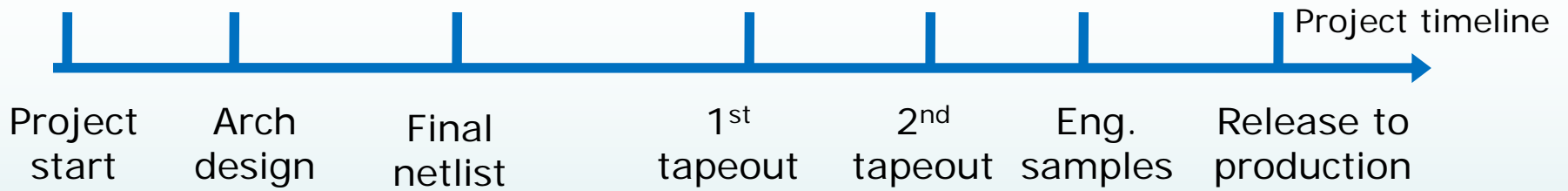
1: Compute IC complexity statistically



A systematic method for calculating complexity calculation is essential

Best-practices throughout project

1 Accurately compute project complexity



2: Estimate resources and schedule—based on models

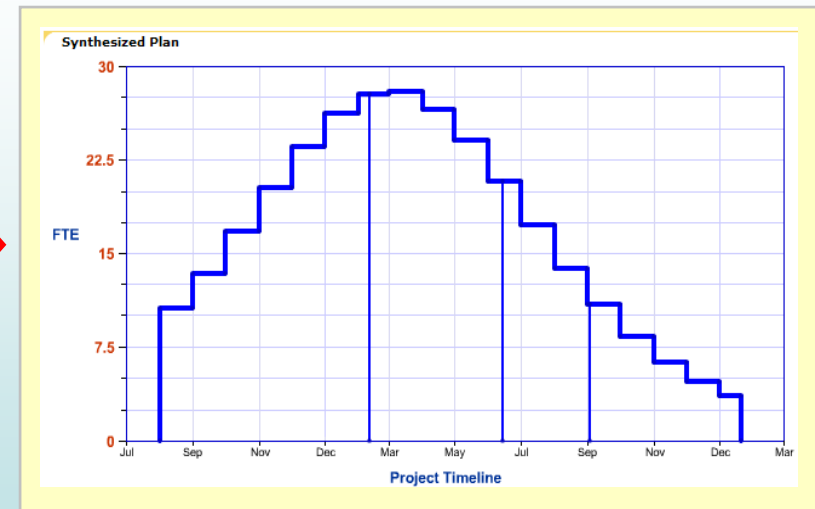
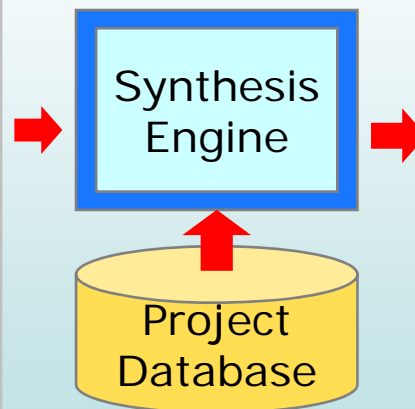
- Accurately estimating project's resources and schedule requires statistical models
- Models help guide intuition and experience

Quick Evaluation of Design Complexity

| | |
|---|---|
| Process Parameters | Processor Cores |
| Min. Process Geometry: <input type="text" value="0.18"/> μm | No. of MPU/MCU/DSPs: <input type="text" value="1"/> cores |
| Avg. Metal Pitch (signal routing layers): <input type="text" value="0.6"/> μm | Digital Logic in All Cores: <input type="text" value="200"/> KGates |
| Total Number of Metal Layers: <input type="text" value="6"/> layers | Memory in All Cores: <input type="text" value="100"/> KBytes |
| Power | Digital Logic (Excluding Processor Cores) |
| Min. Operating Voltage (internal): <input type="text" value="1.2"/> volts | Digital Logic: <input type="text" value="100"/> KGates |
| No. of Supply Voltage Networks: <input type="text" value="3"/> | Memory (Excluding Processor Cores) |
| Timing | SRAM: <input type="text" value="100"/> KBytes |
| Max Clock Frequency: <input type="text" value="2400"/> MHz | DRAM, EEPROM, Flash, ROM: <input type="text" value="1"/> MBytes |
| No. of Independent Clock Domains: <input type="text" value="2"/> | No. of Memory Blocks: <input type="text" value="2"/> blocks |
| No. of Independent Clock Boundaries: <input type="text" value="1"/> <input checked="" type="checkbox"/> | Analog |
| Design Reuse | Analog Circuitry: <input type="text" value="500"/> transistors |
| Digital Logic Reuse: <input type="text" value="Low Reuse"/> | IO Pads |
| Analog Circuitry Reuse: <input type="text" value="High Reuse"/> | No. of I/Os: <input type="text" value="200"/> I/O pads on die |
| Processor Core Reuse: <input type="text" value="High RTL Reuse"/> | |

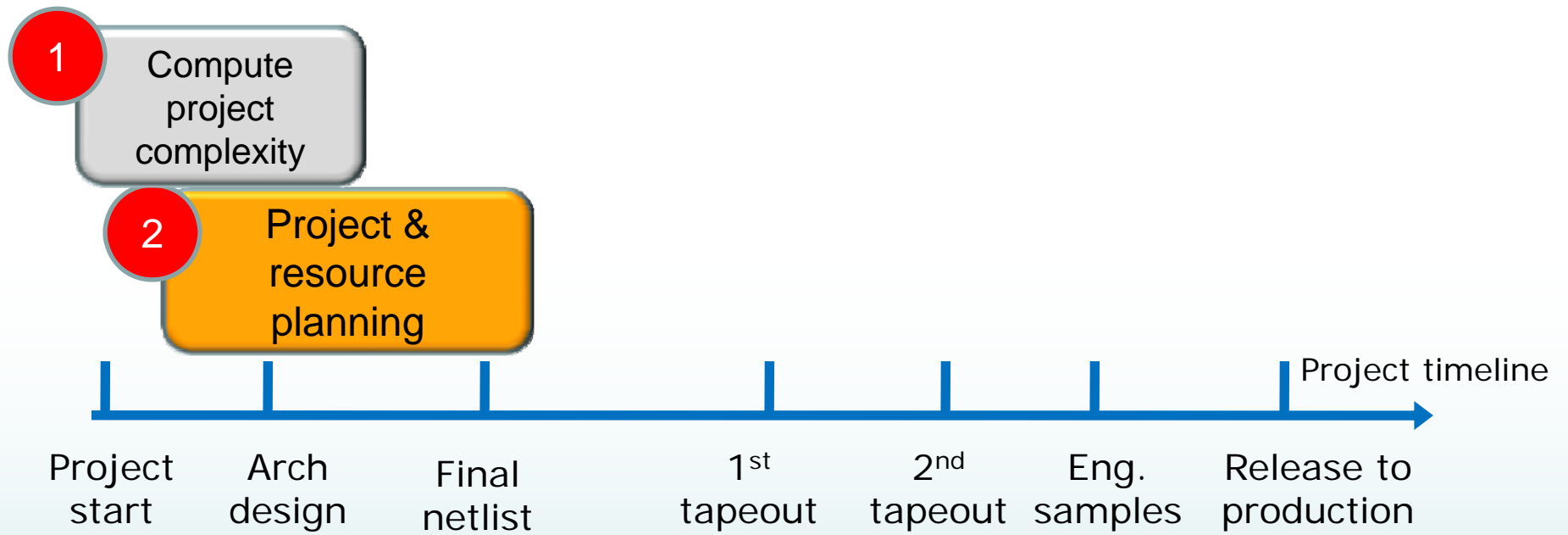
Quick Start Results

Transistor Count: 19,448,309 transistors
Design Complexity: 2,150,502 CUs



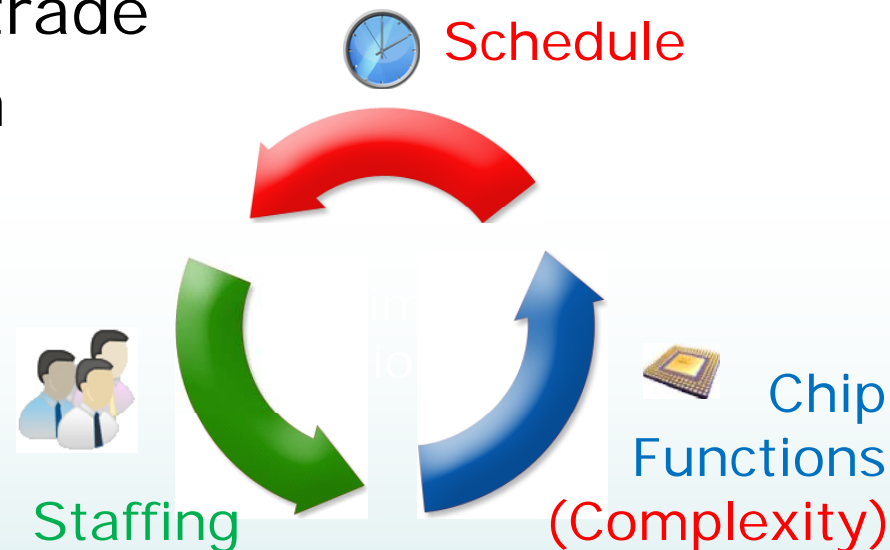
Synthesized Plan Staffing Profile & Timeline

Best practice: resource planning based on models & data



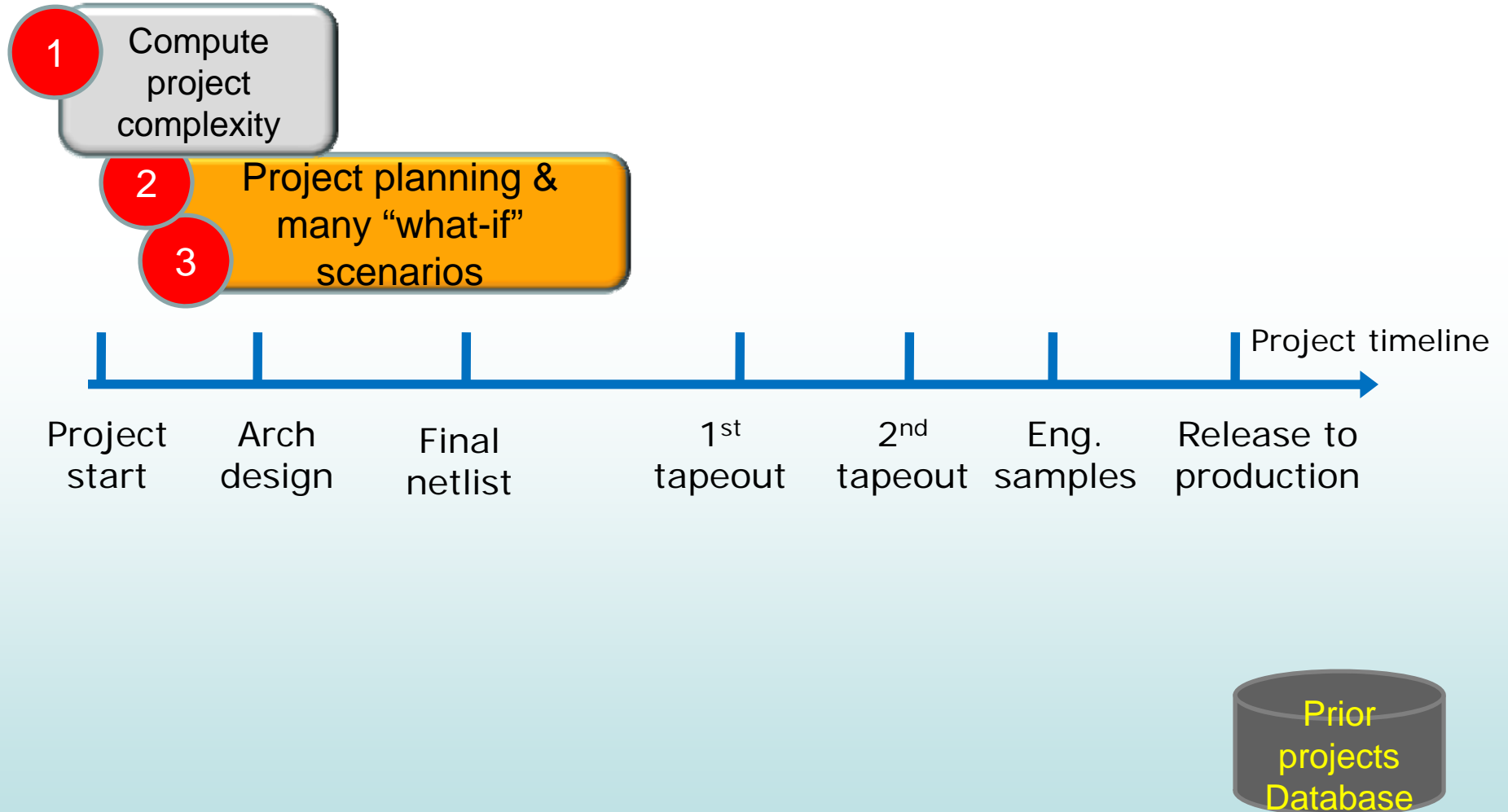
3: Rigorously perform “what-if” scenarios for schedule/resource optimization

- Tools must accurately trade off between project constraints



Ability to generate several scenarios very early in cycle, before settling on one, is extremely powerful

Best practice: do several “what-if” scenarios



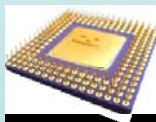
4: Benchmark project execution assumptions

- Benchmark project execution assumptions against your own history and industry data
- Compute your schedule risk given IC complexity, resources allocated and cycle time

Inputs



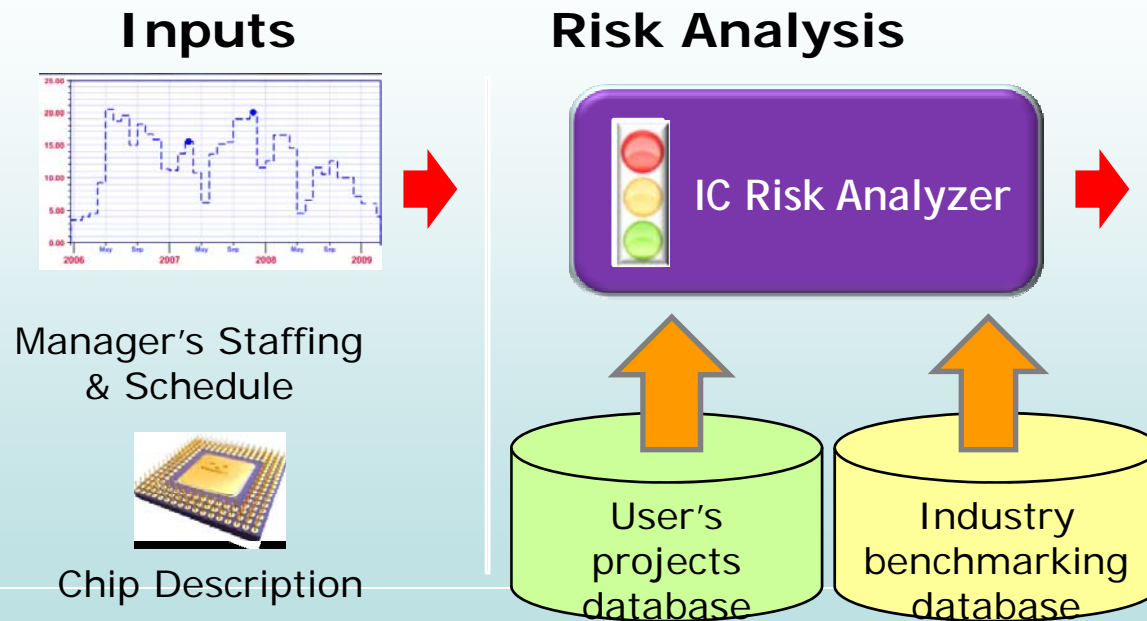
Manager's Staffing
& Schedule



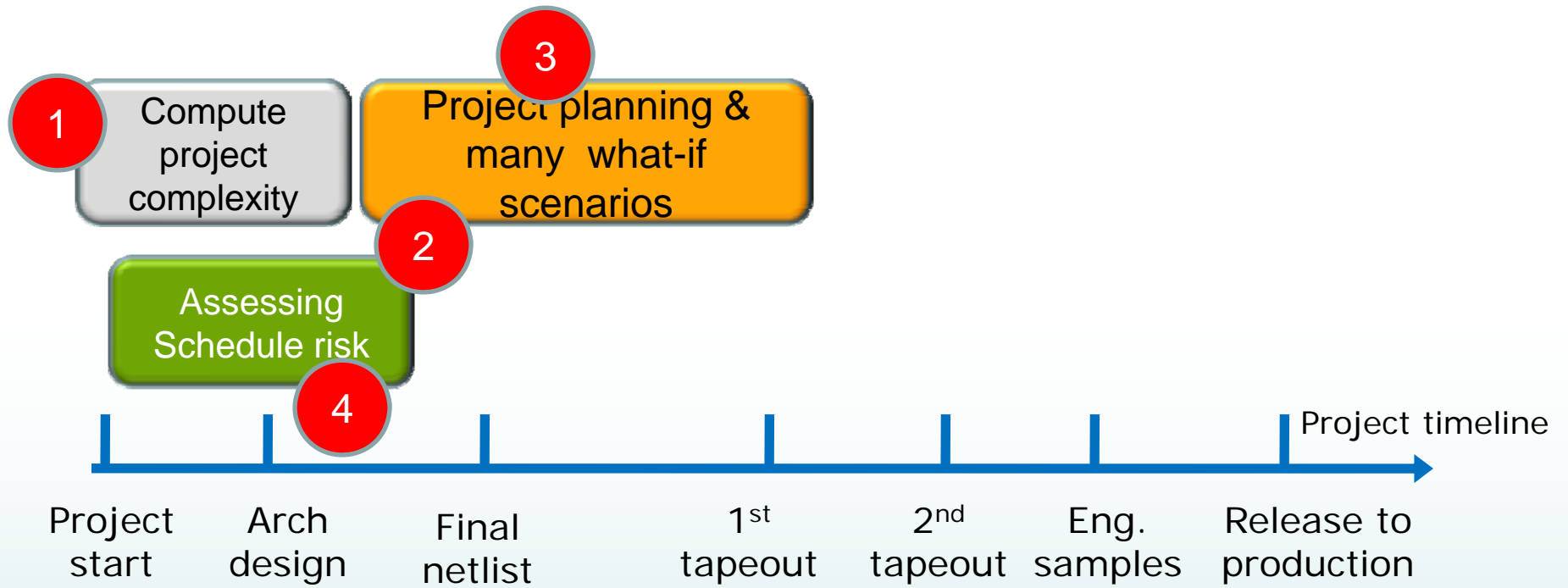
Chip Description

4: Benchmark project execution assumptions

- Benchmark project execution assumptions against your own history and industry data
- Compute your schedule risk given IC complexity, resources allocated and cycle time

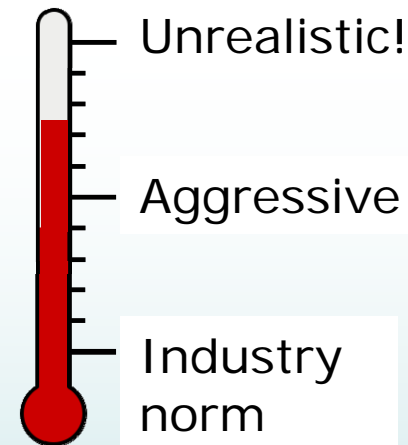


Best practice: benchmark project plan assumptions to compute project risk



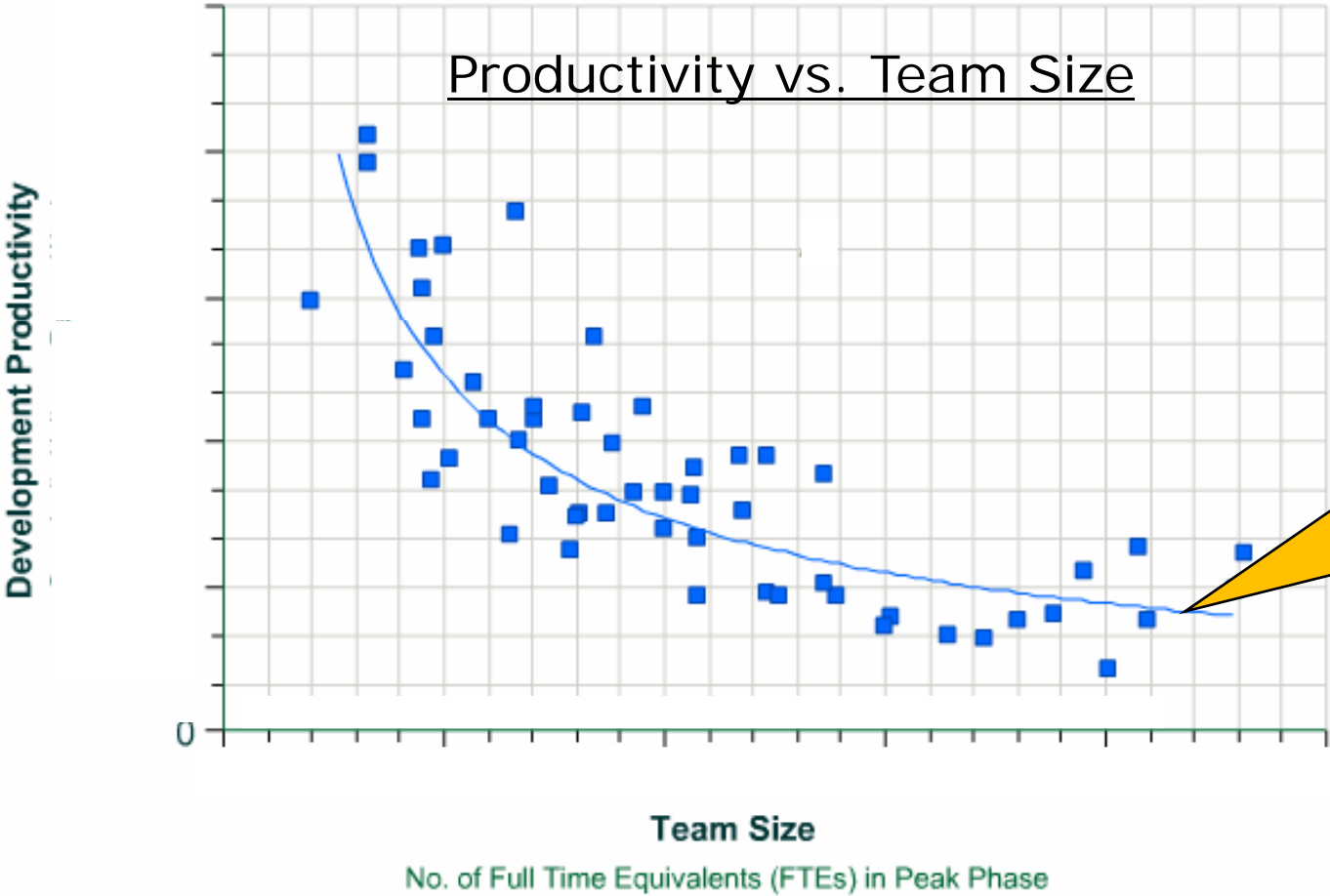
5: Determine most aggressive, *yet achievable*, project plan

- Manager must know what is the highest achievable productivity of his/her team
 - Quantitative
 - Accurate
 - Reliable



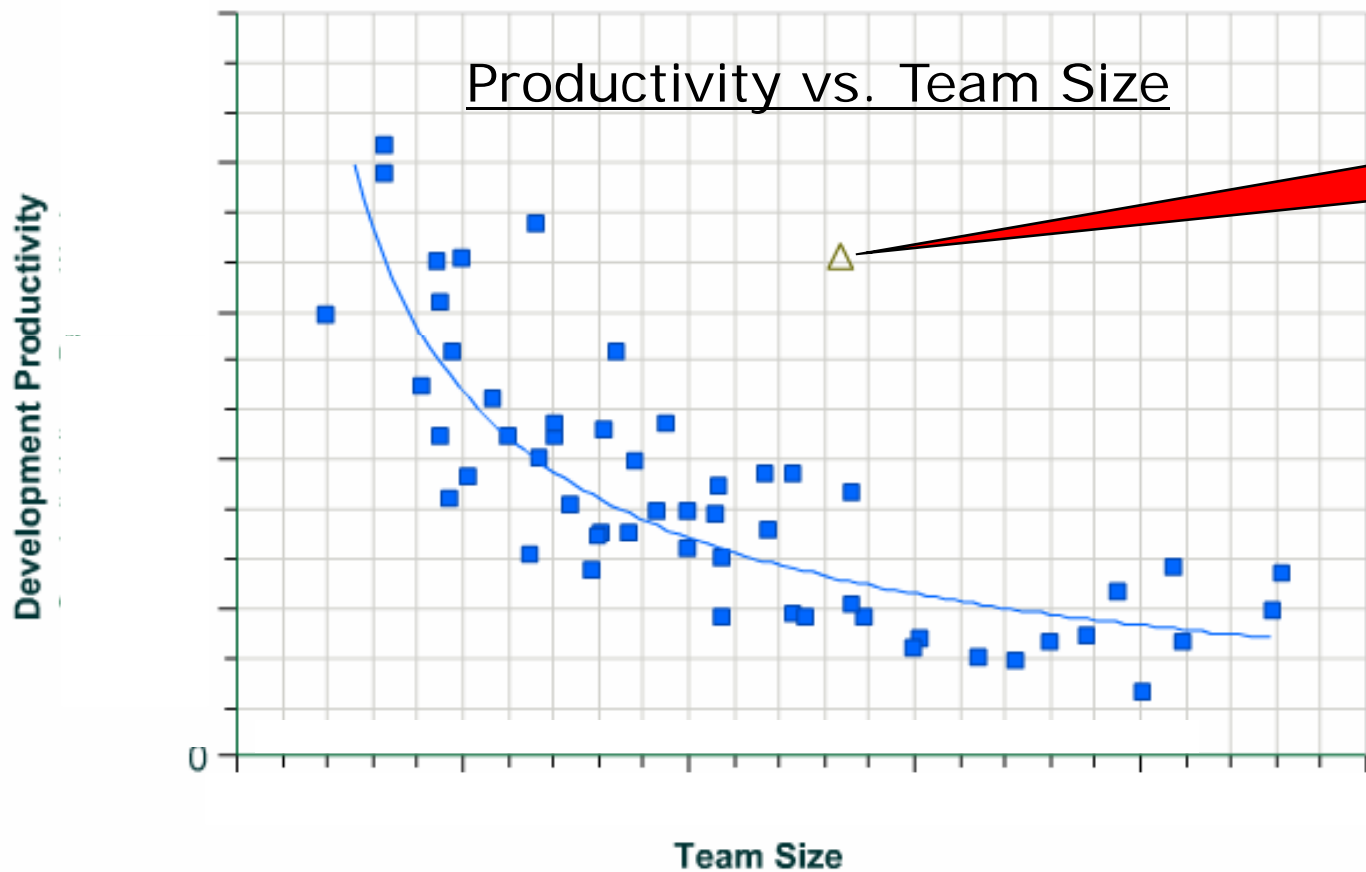
Your Project Plan

Do you know how risky your plan is?



Actual measured productivity levels of teams on similar projects

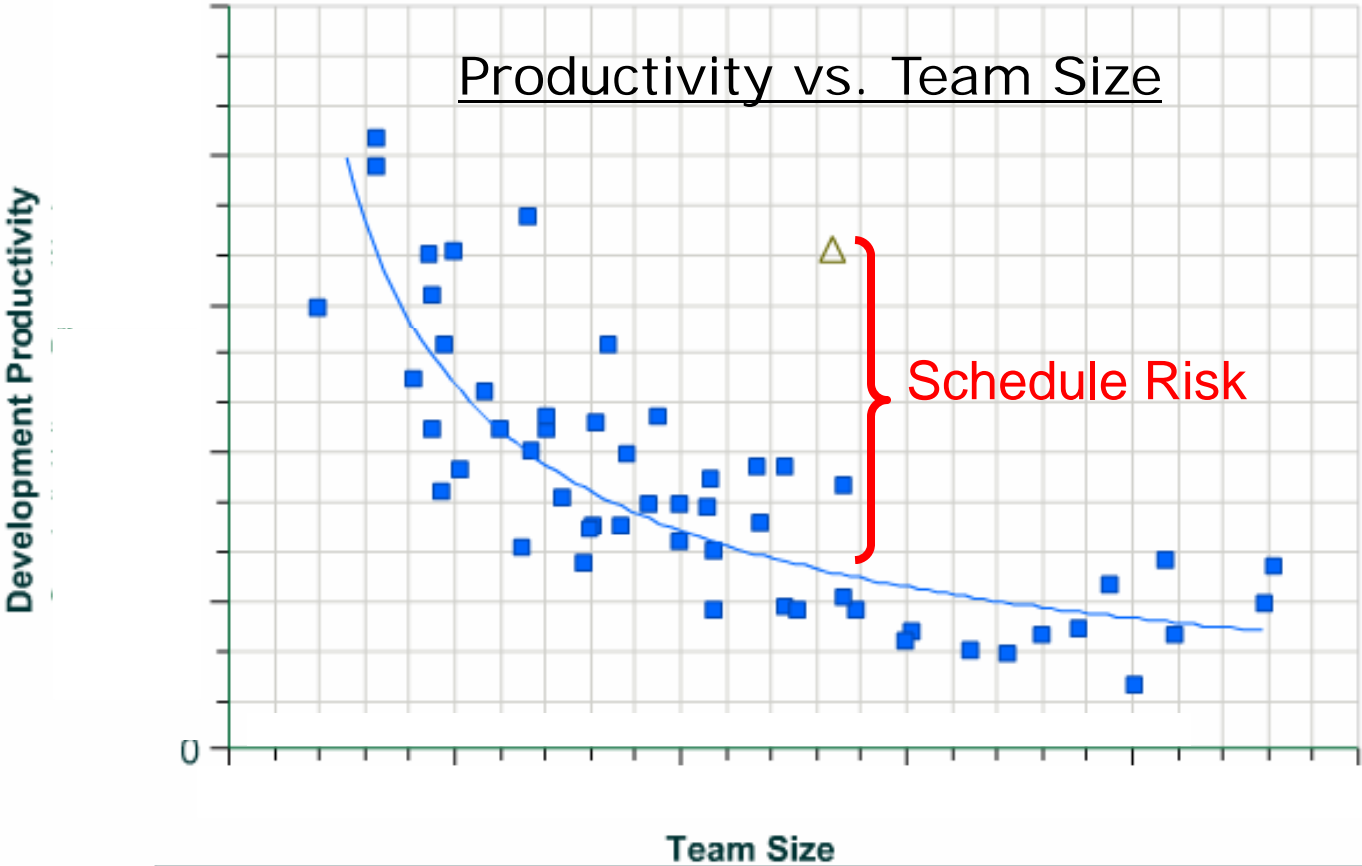
Do you know how risky your plan is?



New project in planning

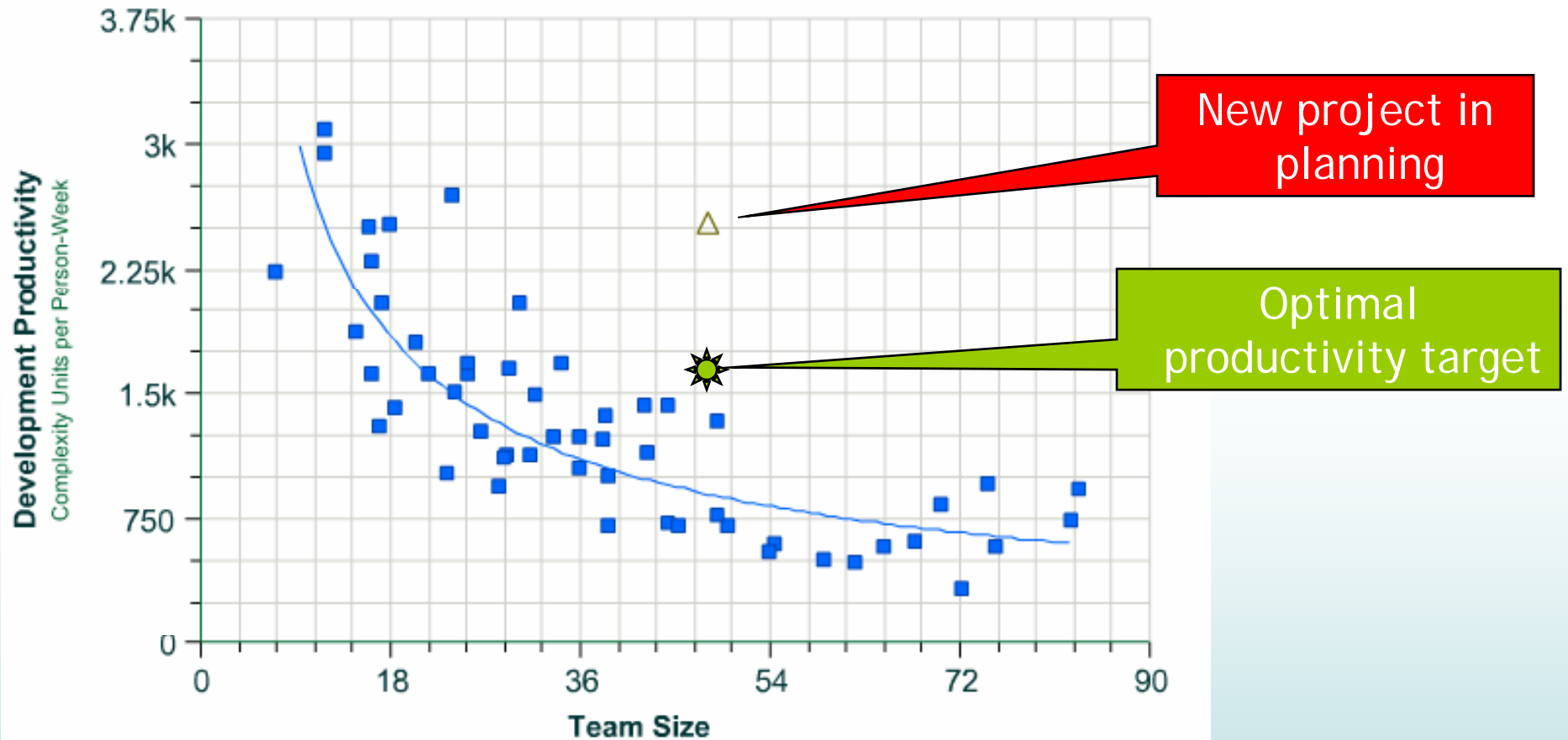
Benchmark assumed productivity in your bottom-up plans

Do you know how risky your plan is?



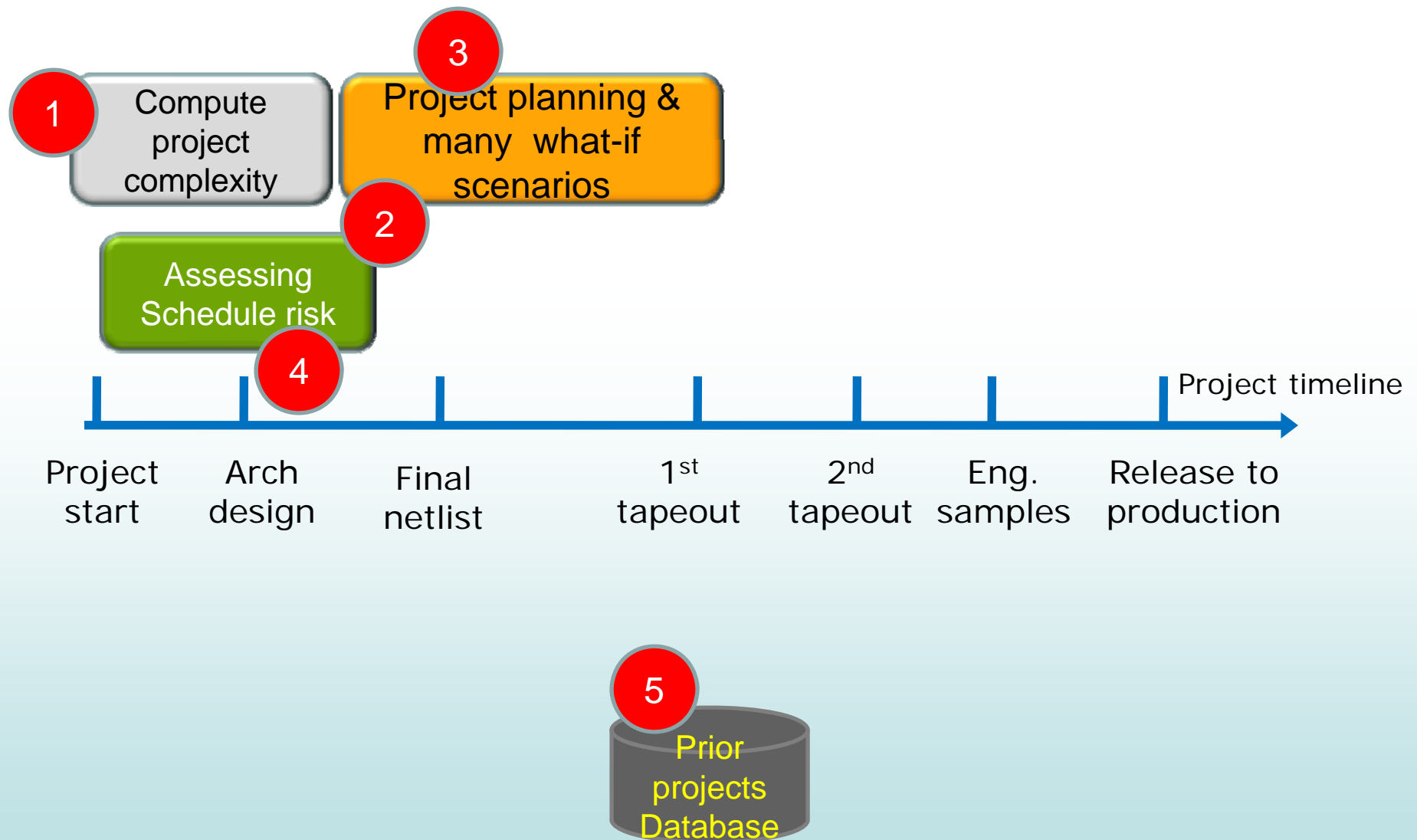
Benchmark assumed productivity in your bottom-up plans

Optimal target: Stretch but don't break



Achieve productivity excellence

Best practice: most aggressive *yet achievable* plan based on database & models

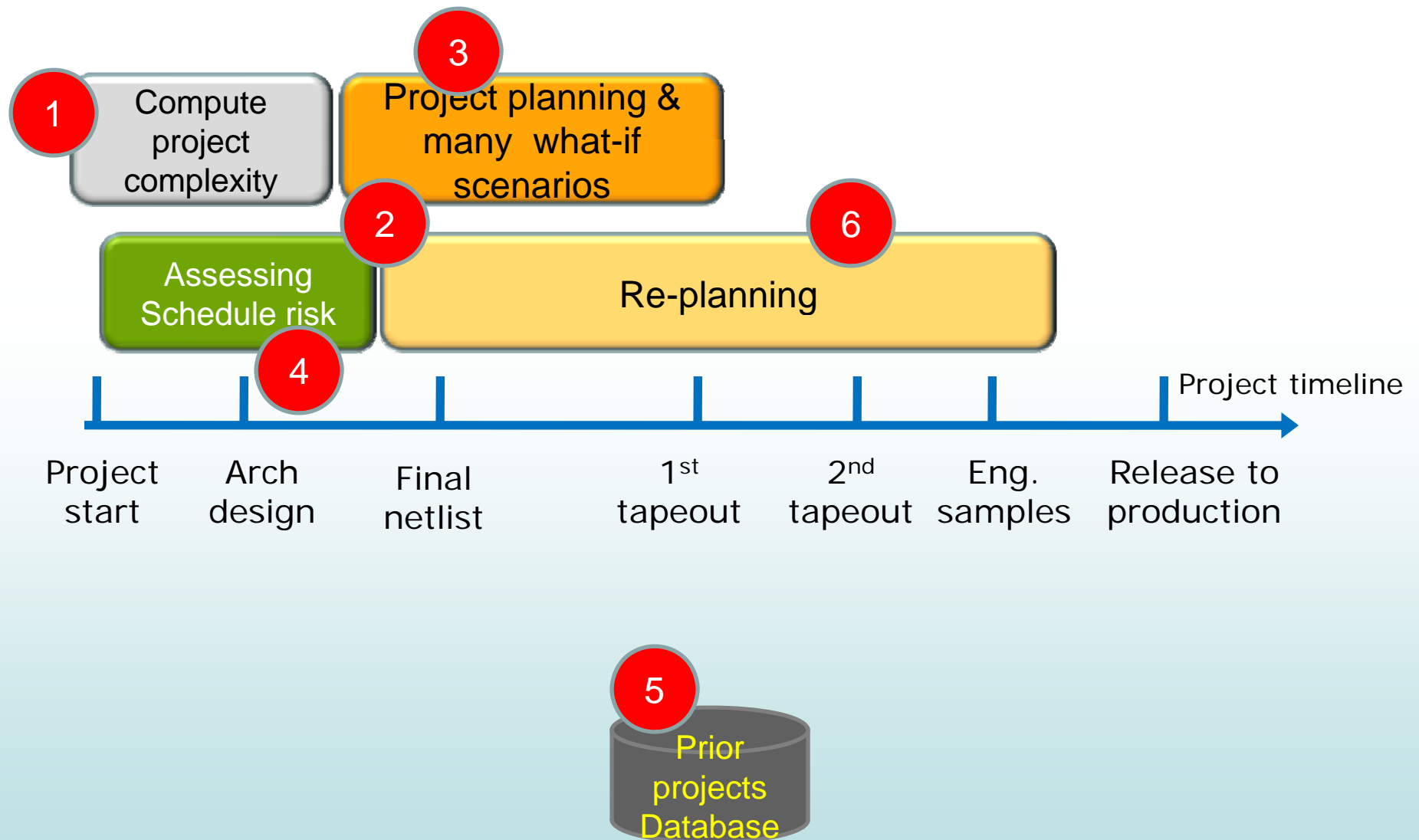


6: Quantitatively assess schedule/resource impact of each feature request

- ↘ Changes are inevitable
- ↘ Re-planning requires a rational discussion of the impact of changes

Compute cost of each request in terms of schedule slips or resources by project phase

Best practice: re-plan based on computed impact



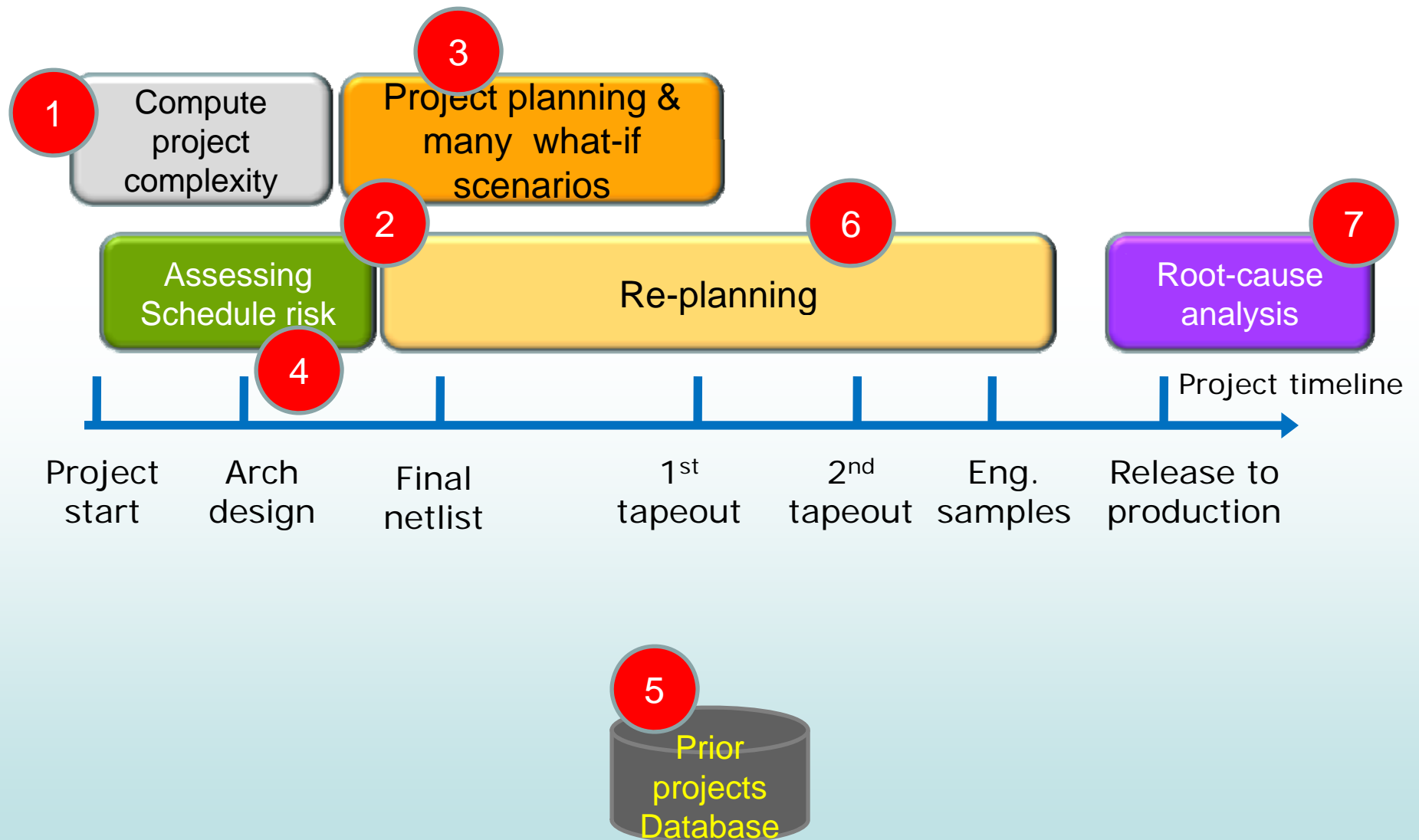
7: Perform root-cause analysis

- Store and organize data from prior projects
- Mine data and extract insight

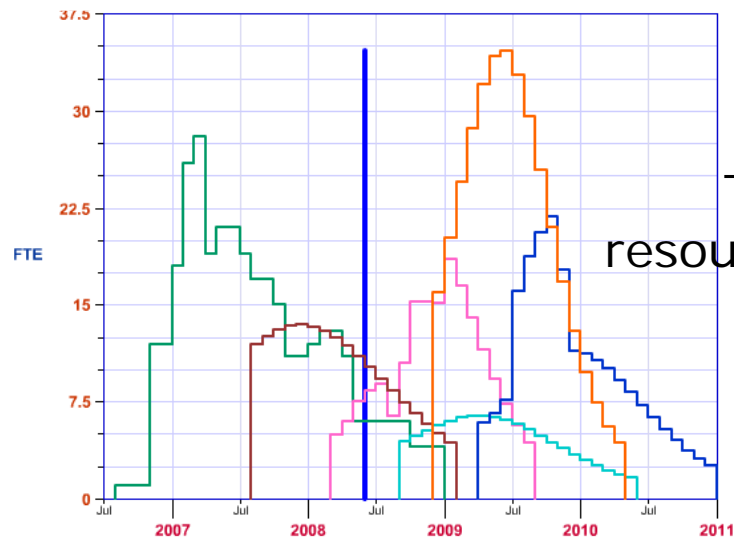
Example of mining the impact of spec stability on schedule slip



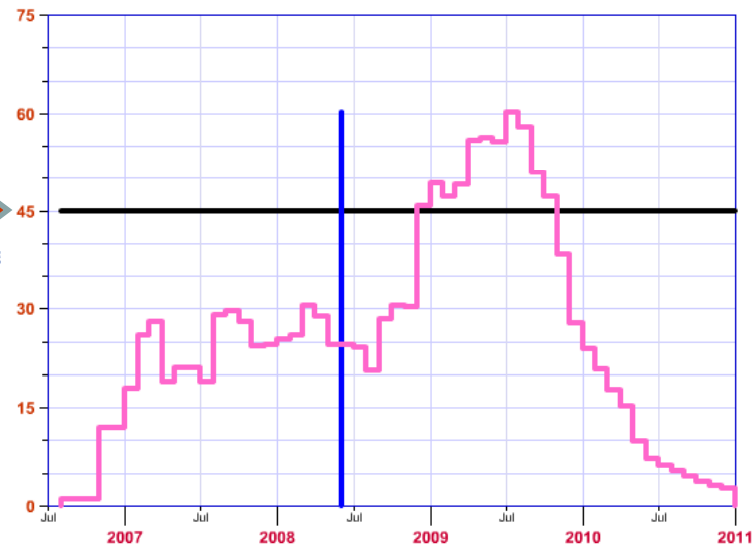
Best practice: rigorous root cause analysis



8: Foresee resource shortfall across pipeline



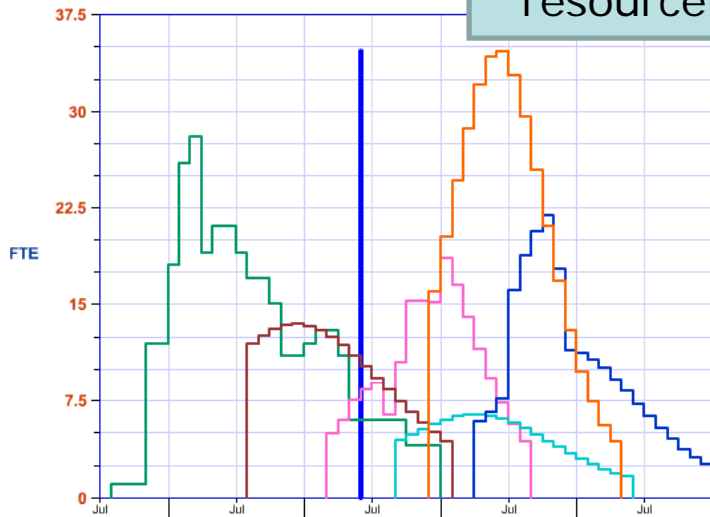
Total resources



today

Identifying and Resolving Resource Conflicts

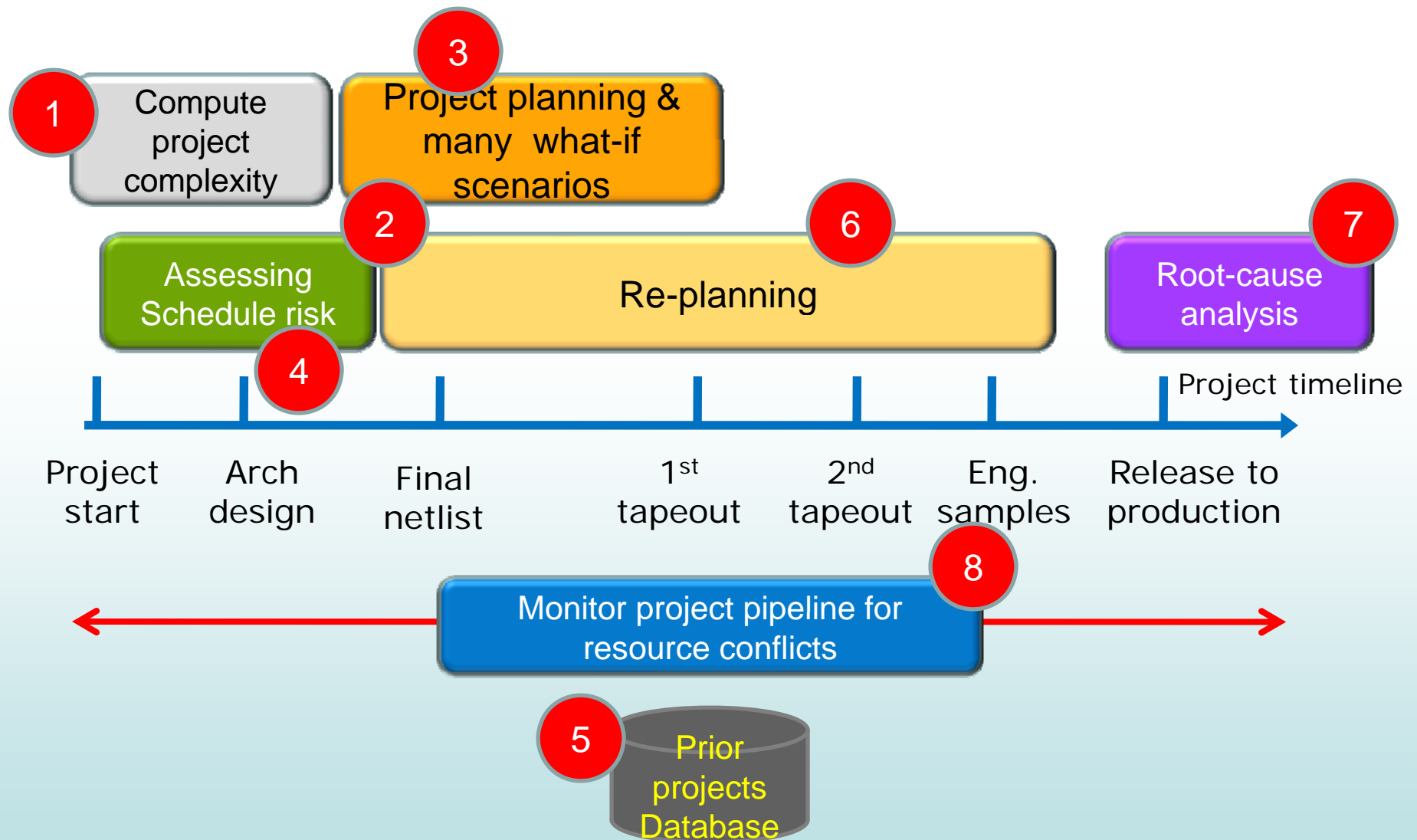
Several projects creating resource crunch 6 months out



| Role | Available FTEs | Peak Demand | | Tolerance | Timeline | | | | | | | | | | | |
|---|----------------|-------------|-----------|-----------|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-----|
| | | Original | Optimized | | b-09 | Mar-09 | Apr-09 | May-09 | Jun-09 | Jul-09 | Aug-09 | Sep-09 | Oct-09 | Nov-09 | Dec-09 | |
| <input type="checkbox"/> Analog Designer | 5.6 | 5.5 | 5.5 | | | | | | 14% | 99% | 91% | 75% | | | | |
| <input type="checkbox"/> Concept Design Engineer | 20.0 | 18.9 | 18.9 | | % | 30% | | 8% | 20% | 15% | 10% | 6% | | | | |
| <input checked="" type="checkbox"/> Gate Level Designer | 8.0 | 10.2 | 10.2 | 2.0 | % | 80% | 80% | 80% | 102% | 60% | 60% | 67% | 81% | 14% | | |
| <input type="checkbox"/> Generic Role | 9.0 | 20.3 | 20.3 | 12.0 | % | 61% | 66% | 72% | 78% | 83% | 87% | 91% | 94% | 96% | 97% | |
| <input checked="" type="checkbox"/> Layout Engineer | 6.0 | 4.2 | 4.2 | 3.0 | | | | 11% | 11% | 35% | 11% | 11% | 23% | 11% | 33% | 47% |
| <input checked="" type="checkbox"/> Logic Verification Engineer | 5.0 | 8.0 | 8.0 | 1.0 | | 33% | 33% | 67% | 80% | 133% | 117% | 129% | 102% | 71% | 67% | |
| <input type="checkbox"/> Other Activities | 30.0 | 25.7 | 25.7 | 5.0 | | | | | | | | 1% | 9% | 30% | 49% | |
| <input type="checkbox"/> Physical Verification Engineer | 8.0 | 8.5 | 8.5 | 0.3 | | | | | | | | 5% | 50% | 45% | 40% | |
| <input type="checkbox"/> Project Manager | 15.0 | 9.0 | 9.0 | | | | | | | | | | | | | |
| <input checked="" type="checkbox"/> RTL Designer | 15.0 | 23.0 | 23.0 | 2.0 | % | 135% | 112% | 114% | | | | | | | | |
| <input checked="" type="checkbox"/> Verification Engineer | 14.0 | 4.0 | 4.0 | 1.0 | | | | | | | | | | | | |
| <input checked="" type="checkbox"/> Overall Team | 37.5 | 55.6 | 55.6 | | % | 138% | 117% | 131% | | | | | | | | |

Cutting one now will save all remaining projects & resource them properly

Best practice: aggressive yet achievable based on data

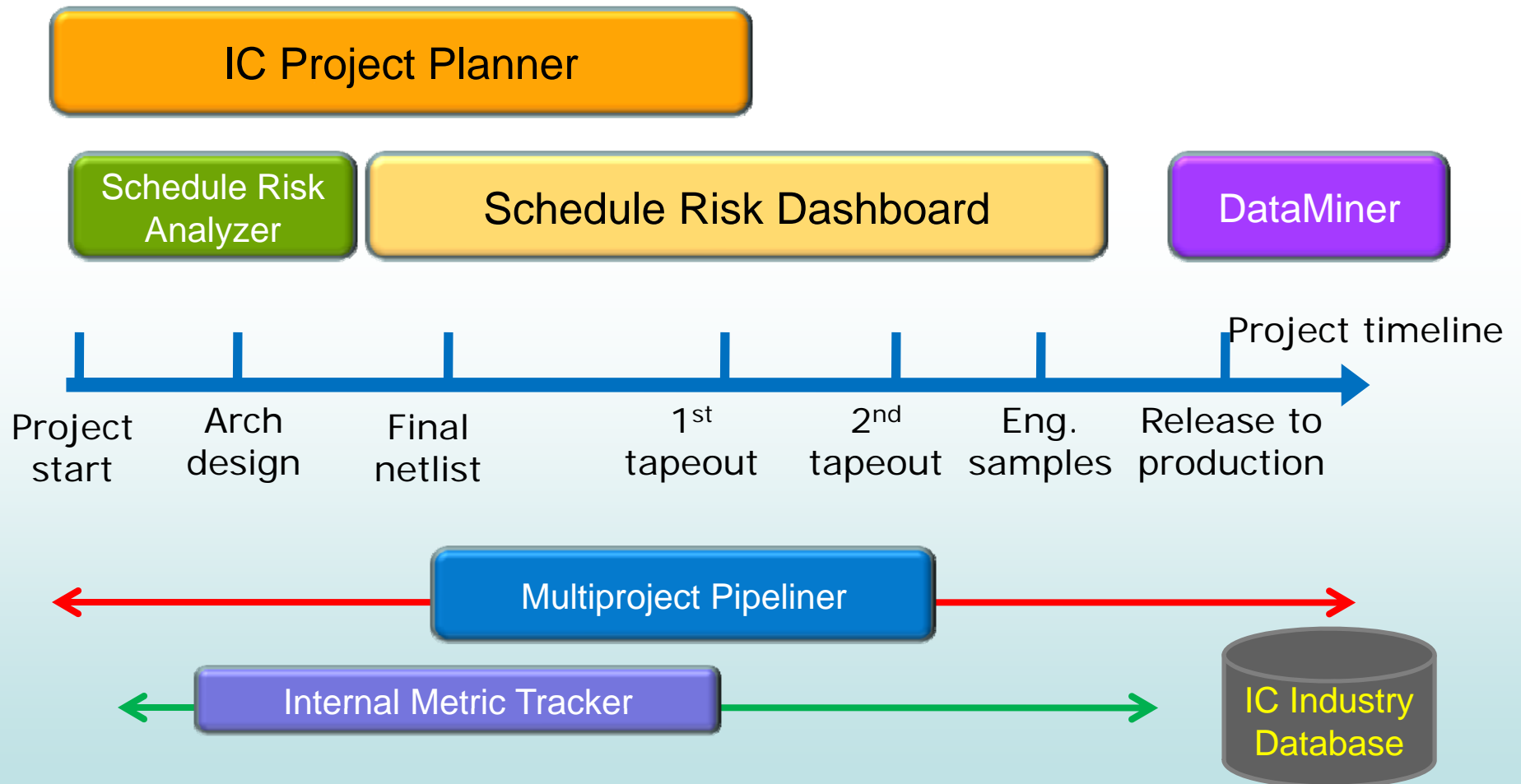


Best practices: Operational disciplines

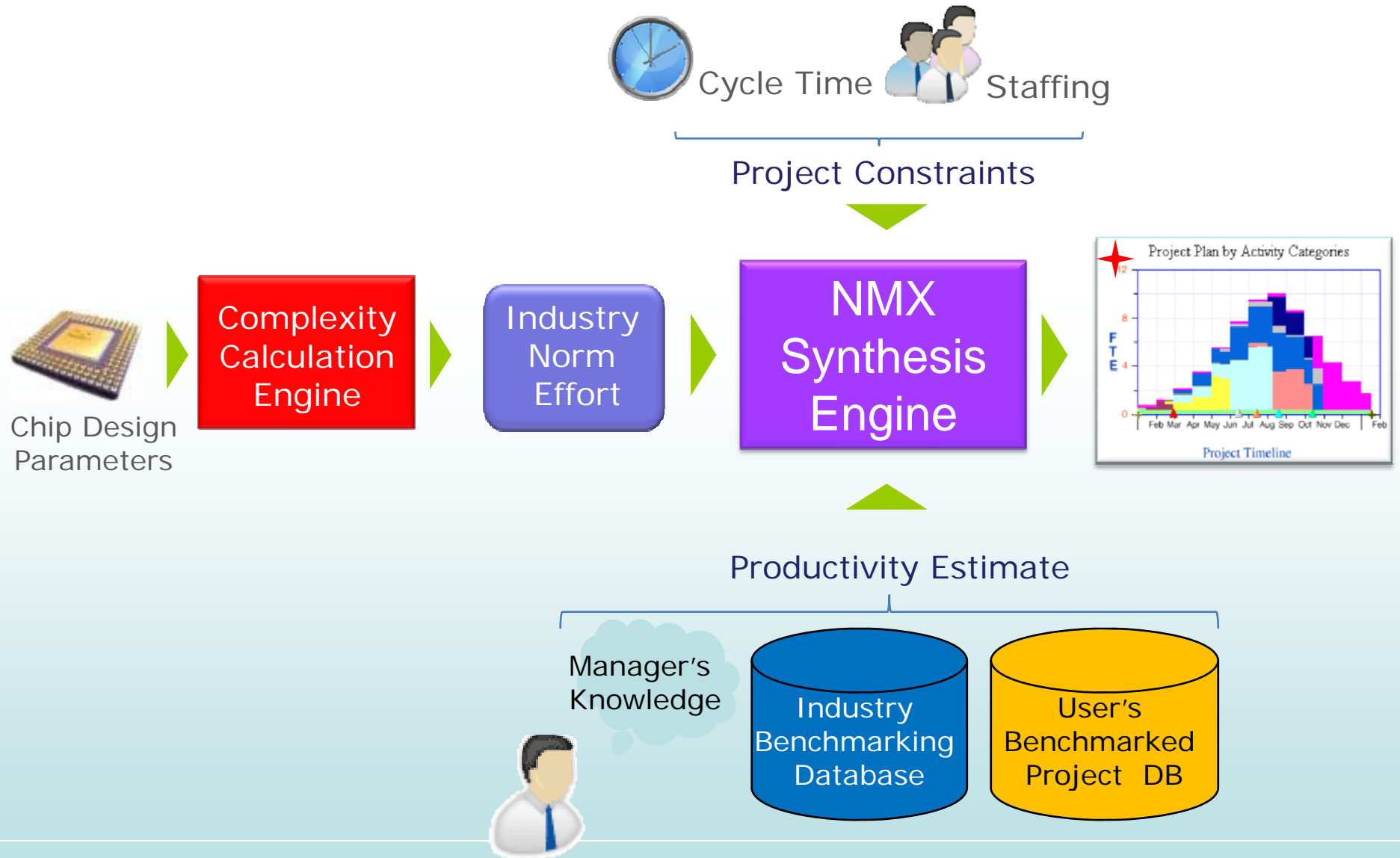
- 1 Compute IC complexity statistically
- 2 Resource planning using models and data
- 3 Generate multiple scenarios using “what-if” analysis
- 4 Benchmark project execution assumptions
- 5 Generate **most aggressive, yet achievable**, project plan
- 6 Quantitatively assess impact of feature changes
- 7 Perform root-cause analysis at project close milestone
- 8 Analyze multi-project execution pipeline to identify resource shortfalls

Numetrics Products for resource planning

Top-Gun tools for the complete project life cycle



NMX IC project planner



Placeholder for demo video

Summary

- Top-gun schedule predictability ends schedule slip
- Top-gun managers create highly competitive schedules *and* achieve them
- Top-gun managers quantify schedule risk early: before bottom-up plans are available
- Numetrics is the solution in daily use at six of the top ten semiconductor organizations today

**To learn more,
download white papers at
www.numetrics.com**