



Press Release

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Underestimating Impact of IP Re-use Can Hurt IC Design Productivity: Numetrics CEO

Ronald Collett to speak at IP-ESC event next month on how to better leverage IP to improve schedule predictability, productivity

Cupertino, Calif.: Nov. 17, 2009 — IC design teams increasingly re-use IP to make the design of large, complex devices more efficient, but they tend to underestimate the work needed to implement the reused IP, causing project delays and missed market opportunities. That's the message Numetrics founder and CEO Ronald Collett will bring to a panel session at IP-ESC 2009 in Grenoble, France, Dec. 1.

Mr. Collett will speak on the panel "IP Reuse vs. IP Leverage: What's the difference, and what are the issues?" The panel will examine how IP deployment is critical for time to market and reduced IC development costs, issues related to verification, deployment, reuse, technology transfer and more.

The panel, to be held at the World Trade Center Congress Area in downtown Grenoble, will be moderated by Kathryn Kranen, president and CEO of Jasper Design Automation, and feature Sanjay K. Srivastava, president and CEO of Denali, and Olivier Haller, who manages the design verification team in the Functional Verification Group at STMicroelectronics, in addition to Mr. Collett.

"It's very difficult to estimate design complexity, especially the impact of reuse," Mr. Collett said. "A leading cause of poor schedule predictability is the inability to estimate the impact of IP modifications on project effort."

Numetrics, which Mr. Collett co-founded, provides a suite of enterprise software tools tailored to the unique needs of system and semiconductor product-development organizations. The company's work with more than 1,500 IC design projects reveals, among other things, the challenge with underestimating the effort needed to implement reusable IP blocks.

Even a small percentage of reuse can add outsized effort to a development project, Mr. Collett said. Adding, for example, one new block of 600,000 gates to a 6 million-gate

design adds 10 percent to the IC but increases the effort required on the project by 24 percent. Adding 10 percent new circuitry to all blocks in that 6 million-gate design—with 90 percent of each block being re-used—doubles the effort required on the project, even though it increases the IC size by just 10 percent to 6.6 million gates.

Mr. Collett will describe ways in which design teams can more accurately measure the complexity of their designs and the impact of design reuse, so they can generate accurate staffing estimates and build more predictable project schedules.

[IP - ESC 2009 \(IP-Embedded Systems Conference\)](#), to be held Dec. 1-3, is the 18th edition of the working conference on hot topics in the design world, focusing for the past eight years on IP-based SoC design. It is held in the renowned Silicon Valley of the French Alps.

Additional Resources

Insight into increasing design productivity can be found in the Numetrics' white papers:

- "Examining the Criteria for Best-in-Class IC Development Process"
(http://www.numetrics.com/downloads/whitepapers/Best_In_Class_new.pdf)
- "Measuring IC Development Productivity"
(http://www.numetrics.com/downloads/whitepapers/MeasuringICDevelopmentProductivity_RC.pdf).

Additional resources are available within the company's online library (<http://www.numetrics.com/about/library.jsp>).

About Numetrics Management Systems, Inc.

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