



Press Release

Numetrics Contact: Brian Fuller

brian.fuller@numetrics.com

Numetrics CEO: Misunderstanding Project's True Cost Can Doom SOC Design Efforts

Ronald Collett, speaking on EE Times virtual panel, says project success can be achieved by quantifying design complexity to understand schedule risk

Cupertino, Calif: Sept. 22, 2009—Profitable system-on-chip (SOC) designs require engineering managers to understand the true development cost of their products so they can manage resources effectively and exploit market opportunities.

That was the assessment of Numetrics' CEO Ronald Collett, who participated on the panel "Economics of Next Generation SOC Design: A Node Too Far?" during the online EE Times SOC Virtual Conference Sept. 16. The panel and the event—which reported record live attendance—are now available in archived form by clicking on <http://www.eetimes.com/soc/>.

Mr. Collett joined three other industry executives on the panel— Steve Douglass, vice president, product development, Xilinx, Grant Martin, chief scientist, Tensilica Inc., and Sven Andersson, ASIC FPGA designer, Realtime Embedded AB—to discuss the challenges of electronics design in the coming years. EE Times Online Editor Dylan McGrath moderated.

"You reach a point where it's no longer justifiable to invest in an SOC. If the design costs \$50 million to \$80 million to develop, and there's only a \$200 million market opportunity for the device, then the design can't be justified," Mr. Collett said during the event. "Getting your arms around true development cost is what SOC development is all about."

Half of development costs are engineering resources, and companies historically underestimate the effort and cost required to complete projects on time, he added. But quantifying design complexity and effort, assessing staffing requirements based on industry norms and running informed what-if analyses ensure insight into whether the project is right for the market opportunity, Mr. Collett said.

Mr. Collett co-founded Numetrics, which provides a suite of enterprise software tools tailored to the unique needs of system and semiconductor product-development organizations.

Insight into increasing design productivity can be found in the Numetrics' white papers:

- "Examining the Criteria for Best-in-Class IC Development Process"
(http://www.numetrics.com/downloads/whitepapers/Best_In_Class_new.pdf)
- "Measuring IC Development Productivity"
(http://www.numetrics.com/downloads/whitepapers/MeasuringICDevelopmentProductivity_RC.pdf).

Additional resources are available within the company's online library (<http://www.numetrics.com/about/library.jsp>).

About Numetrics Management Systems, Inc.

Numetrics (www.numetrics.com) provides a suite of software tools tailored to the unique needs of the R&D organizations in semiconductor and systems companies. The enterprise resource planning (ERP) software enables unprecedented predictability of chip development schedules, reliably measures project schedule risk and benchmarks product development performance against the industry's best-in-class. The company is headquartered at 20863 Stevens Creek Boulevard, Suite 510, Cupertino, Calif. Numetrics Management Systems is a trademark of Numetrics Management Systems, Inc. All other brands or products are the trademarks or registered trademarks of their owners.